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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,843	07/21/2003	Veronika Polei	P2002,0618	6526

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/623,843	POLEI ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-7* is/are allowed.

6)☒ Claim(s) *1-3 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Alsmeier et al. (U.S. Patent 5,627,092).

In re claim 1, **Alsmeier** discloses a method for fabricating a buried bit line for a semiconductor memory, which comprises:

providing a semiconductor body **36** (col. 3, lines 14-23 and FIG. 4.1);

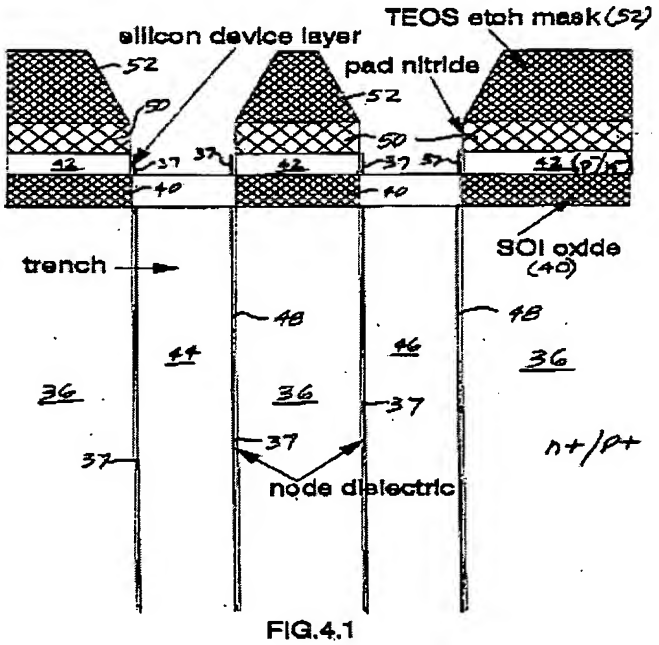

FIG.4.1

applying a lower boundary layer **40** and a storage layer **50** to the semiconductor body **36** (col. 3, lines 25-35 and FIG. 4.1);

applying a sacrificial layer **52** made from a material selectively etchable with respect to the storage layer **50** and to polysilicon onto the storage layer **50** (col. 3, lines 25-35 and FIG. 4.1);

producing openings **44, 46** in the sacrificial layer **52**, the storage layer **50**, and the lower boundary layer **40**, extending to the semiconductor body **36**, the openings **44, 46** being produced above regions where buried bit lines are to be produced (col. 3, lines 14-35 and FIG. 4.1);

introducing doped polysilicon **54** into the openings **44, 46** (col. 3, lines 36-46 and FIG. 4.2);

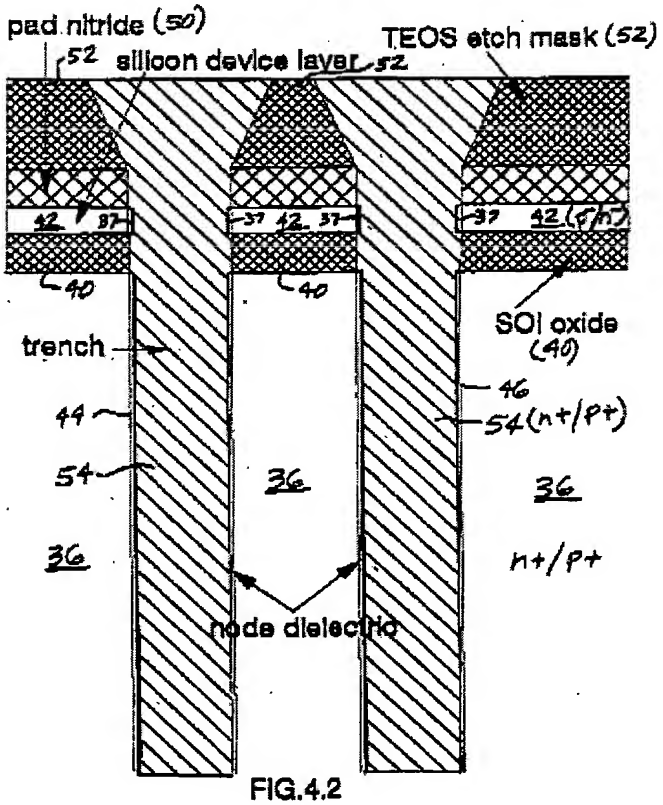

FIG.4.2

etching back the polysilicon **54** to a residual portion (col. 3, lines 42-46 and FIG. 4.4);

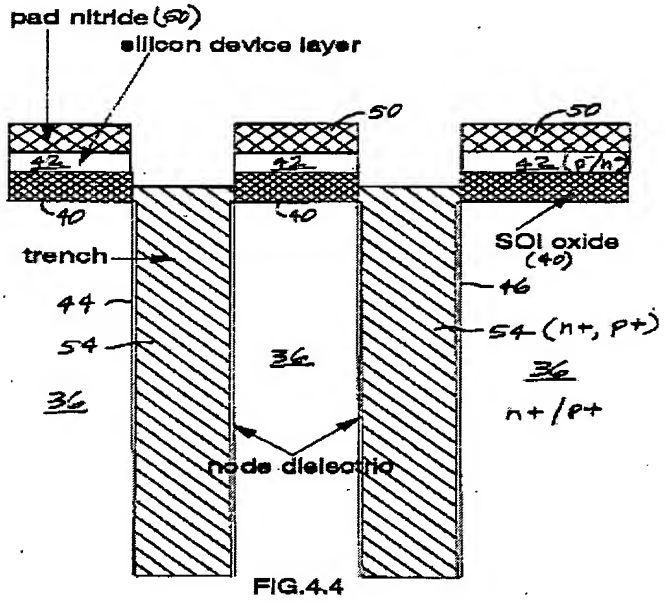

FIG.4.4

removing the sacrificial layer **52** (col. 3, lines 40-41 and FIG. 4.3);

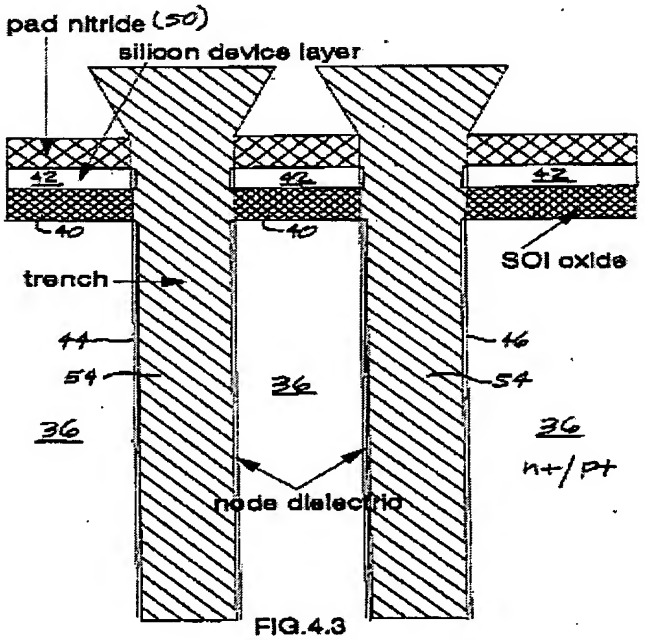

FIG.4.3

applying an upper boundary layer **58** on the surface of the storage layer **50** and the residual portion of the polysilicon **54** and oxidizing the residual portion of the polysilicon to form an oxide region, the oxide region being thicker than the lower boundary layer **40**, the lower boundary layer, the storage layer and the upper boundary layer acting as a gate dielectric (col. 3, line 47 to col. 4, line 5 and FIGS. 4.7-4.8);

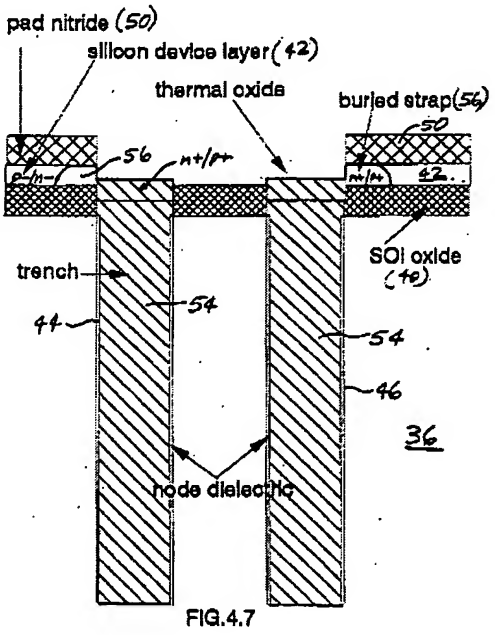

FIG.4.7

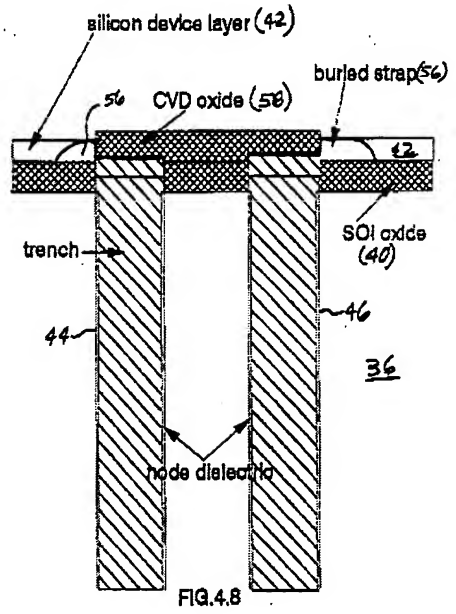

FIG.4.8

forming a diffusion region in the semiconductor body below the oxide region during the oxidation of the residual portion of the polysilicon, the diffusion region forming the buried bit line (col. 3, lines 56-65).

In re claim 2, **Alsmeier** discloses that the sacrificial layer **52** is produced as a deposited oxide (col. 3, lines 36-41).

In re claim 3, **Alsmeier** discloses that the method according to claim 1, which further comprises selecting the storage layer **50** from a group of material consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide,

zirconium oxide, aluminum oxide, and intrinsically conductive silicon (col. 3, lines 24-34).

In re claim 8, **Alsmeier** discloses that the method according to claim 1, which further comprises producing spacers **48** at walls of the openings before introducing the polysilicon **54** into the openings **44, 46** (col. 3, lines 34-41 and FIGS. 4.1-4.2).

Allowable Subject Matter

Claims 4-7 are previously allowed.

Response to Applicants' Amendment and Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Applicants contend that no portion of the polysilicon filing is oxidized in the method of Harak et al. (U.S. Patent 6,063,658) herein known as Harak.

In response to Applicants' contention that no portion of the polysilicon filing is oxidized in the method of Harak. Examiner respectfully submits that Applicants' argument is moot in view of the newly discovered reference to Alsmeier et al. (U.S. Patent 5,627,092) applied under 35 U.S.C. 102(b) rejection in the necessitated new ground(s) of rejection presented in this Office Action. Specifically, Alsmeier discloses oxidizing the residual portion of the polysilicon to form an oxide region, the oxide region being thicker than the lower boundary layer 40, the lower boundary layer, the storage layer and the upper boundary layer acting as a gate dielectric (col. 3, line 47 to col. 4, line 5 and FIGS. 4.7-4.8);

For this reason, Examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
October 25th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER